

REMARKS

This is intended as a full and complete response to the Final Office Action dated October 12, 2007, having a shortened statutory period for response set to expire on January 12, 2008. Applicants submit this response to place the application in condition for allowance or in better form for appeal. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-22 are pending in the application. Claims 1-22 remain pending following entry of this response. Claims 1-4, 16-18 and 22 have been amended. Applicants submit that the amendments do not introduce new matter.

Claim Rejections - 35 U.S.C. § 103

Claim 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Haupt* (U.S. Patent No. 6,334,159) and further in view of *Halbert et al.* (U.S. Patent No. 6,317,352, hereinafter, "*Halbert*").

Applicants respectfully traverse this rejection.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. See MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See MPEP § 2143. The present rejection fails to establish at least the third criteria.

In this case, *Haupt*, in view of *Halbert*, does not disclose "each and every element as set forth in the claim." For example, regarding claim 1, *Haupt* does not teach a plurality of command segments with a respective plurality of elements, wherein one of the command segments is a selection command segment for selecting at least two memory banks of a memory module. Claims 16 and 22 disclose similar limitations.

Haupt simply discloses a Symmetrical Multi-processor System (SMP) System Platform 100, as illustrated in FIGs. 1-3, wherein a plurality of processing modules (PODs) (120A, 120B, 120C, 120D), interface with multiple memory storage units (MSUs) (110A, 110B, 110C, 110D). Each MSU comprises a memory controller 550 that is coupled with memory clusters (535A, 535B, 535C, 535D) via address buses (570A, 570B, 570C, 570D) and a control bus (640A). Each memory cluster (535A, 535B, 535C, 535D) may comprise “arrays of SDRAM devices” (See *Haupt*, col. 7, Lines 2-4) that are stored in a directory storage array (630A, 630B). Consequently, *Haupt* only discloses the function and behavior of the control and address signals used to select between the memory clusters (as illustrated in FIGs 2 and 3). Nowhere is the functionality and behavior disclosed for address and control signals that are for selecting at least two memory banks of the SDRAM devices. This level of granularity is simply not disclosed in *Haupt*. Therefore, *Haupt* does not teach a plurality of command segments with a respective plurality of elements, wherein one of the command segments is a selection command segment for selecting at least two memory banks of a memory module.

Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 1, 16, 22, and the claims that depend therefrom.

Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

If the Examiner believes any issues remain that prevent this application from going to issue, the Examiner is strongly encouraged to contact the undersigned attorney to discuss strategies for moving prosecution forward toward allowance.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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